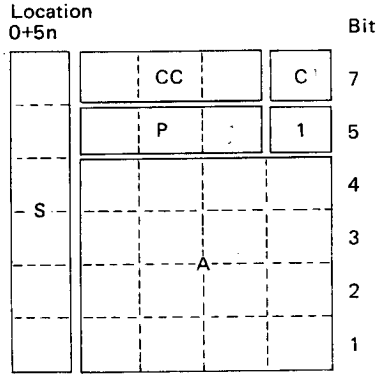
P, B and A registers

The P, B and A registers reside in protected Common (locations 0 to 299):

P register	locations 0 to 99
B register	locations 100 to 199
A register	locations 200 to 299

Each register is divided into 20 sections, one per partition. The starting location for each partition register is found from M+5n, where M is 0(P), 100(B), 200(A), and n is the partition number.

Each P register contains the return program address and other related information.



P register bit layout

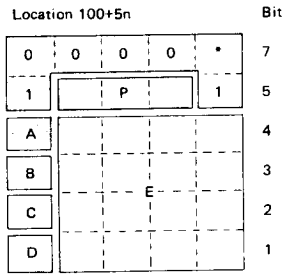
C = address bit
0 = partition and 1 = Common
S = partition size
blank = absent
0 to 9 = core size in 1000's
: = 10K (or more on Model 22)
A = address of next instruction to be executed
P = page indicator bits
CC = condition code bit configurations

Note: cc = 4 occurs only with cc = 1, 2 or 3.

Condition code settings	Bit settings in CC field		
1	*	1	0
2	*	*	1
3	*	0	0
4	1	*	*

*Bit may be 0 or 1

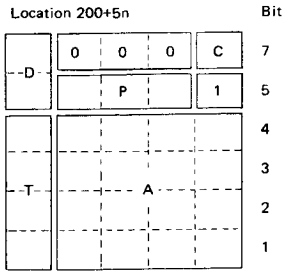
Each B register contains the I/O character counter and activity information.



B register bit layout

A = I/O active when 1, inactive when 0
B = non-fill when 1, fill when 0
C = control when 1, normal when 0
D = write when 1, read when 0
E = residual character count minus one
(will be 9999 when count is exhausted)
P = page indicator bits
Unused bit (*) may be 0 or 1

Each A register contains the next I/O address and the FAC protection character.



A register bit layout

C = address bit
0 = partition and 1 = Common
A = next I/O core address
P = page indicator bits
D = disc access mask. (When bit 7 = 0 and bit 5 = 0, read and write operations are permitted.
When bit 7 = 0 and bit 5 = 1, read only is permitted.
When bit 7 = 1 and bit 5 = 0, read and write permitted from Common only. When bit 7 = 1 and bit 5 = 1, no access is permitted).
T = tape access mask where bits 1 to 4 correspond to devices 1 to 4.
(Tape access is permitted only when bit = 0.)